REMARKS

[§ 112] Claims 1-8 and 16-19 were rejected under §112 on the basis of "in" and "on." This rejection is respectfully traversed.

The Examiner is understood to hold that in claim 1 "in" implies a location *under* the surface. The Applicant respectfully disagrees. Claim 1 recited a surface; the surface comprising regions; the regions including a wiring region "in which wirings ... are formed." Clearly, "in" refers back to the surface and expresses a location *on* the surface. A surface has no depth, so a thing that is referred back to the surface can be elsewhere than *on* the surface. In a Venn diagram, one region may be *in* another but both are still *on* the surface of the paper.

The Examiner states on page 7 of the Action that the Applicant's arguments are moot in view of the new grounds of rejection, but the present rejections under §§102-103 are exactly the same as in the previous Action. Therefore, the new grounds of rejection is that of the rejection under §112.

However, the rejection under §112 is made over language that was not changed by the previous Amendment. For example, "*in* which wirings ... are formed" was in claim 1 prior to the RCE Amendment. Furthermore, the Applicant's arguments in the previous Amendment clearly showed that *on* the surface was the intended meaning in regard to the wiring.[1]

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[1] The Applicant earlier argued:

"As is explained in the Applicant's specification at the top of page 7, the exemplary wirings 18 (Fig. 1) are confined to the wiring region 28 (Fig. 2), and they and the chip region 30 are surrounded by the exemplary reinforcement layer region 32 (Fig. 2), with its reinforcement layer 20 (Fig. 1).

"As the Examiner notes (line 5 of ¶ 3 on page 2), Baba does not illustrate the claimed wiring region, but the Examiner asserts that wiring is under the chip 1 in Fig. 5B. The Applicant agrees that wiring must be there; the internal wiring appears to extend internally throughout the substrate, because Baba states that the wiring connects the electrodes 7 and 12 (col. 1, lines 58-60) and the electrodes 12 extend to the outer edge of the substrate. However, the wiring is inside the board 4 (except for the chip region of the top surface) and not **on** the surface. There is no surface wiring region.

"In contrast, the Applicant claims non-overlapping reinforcement and wiring regions and layers **on** the surface of the insulating substrate. Instant Fig. 2, for example, shows that the wiring regions 28 the reinforcement region 16 do not overlap each other. Reinforcement layers 20 are not provided on top of the wirings, as in Baba.

"The advantage of the Applicant's claimed feature is that the reinforcement layers can be formed at the same time as the wirings. Therefore, reinforcement layers can be introduced into the structure without an additional manufacturing step (e.g., without any additional lithography).

"A further advantage is that the surface of the solder resist 22 (the protective film) is substantially flat over the chip region, since both of the wiring region and the reinforcement region do not overlap with the chip region. This prevents a so-called "void" from being generated in the solder resist (protective film). Thus, the reliability of the

By the remarks above, the Applicant believes that the present rejection was not necessitated by the Applicant's amendment, and, therefore, the next rejection should not be final.

The Examiner stated on page 7 of this Action that the Applicant's previous arguments are moot "in view of the new grounds of rejection" (i.e., the formal rejection). The Applicant respectfully protests this statement. The Applicant's arguments should be given full weight unless they clearly and unambiguously do not refer to the claim language, and that was certainly not the case here.

Claim 9, which was not rejected under §112 (and is not amended), recites "wirings provided in the second region *on the top surface* of the insulating substrate"—it unambiguously recites wiring that is not under the surface. However, claim 9 was and is rejected along with claims 1 and 6 under §102. The Applicant notes that if the present rejection is indeed based on "in" and "on," and the Applicant understand, then the rejection is inconsistent.

The claims are amended to further clarify the Applicant's meaning. Withdrawal of the rejection is requested.

[§102] Claims 1-3, 6, 9, 12, 13, and 15-18 were rejected under § 102 as being anticipated by Baba '077. This rejection is respectfully traversed.

(1) The Applicant reiterates that Baba does not disclose wiring on the surface. As mentioned above, the Applicant believes that the claim language does, and did, clearly distinguish over Baba, which shows wiring only *under* the surface.

Claim 9 (which was not rejected under §112) recites "wirings provided in the second region *on* the top surface of the insulating substrate" and is most clear in reciting wiring that is not under the surface. Amended claims 1 and 6 are now perfectly clear on the same point, even if they were not before this amendment (not admitted).

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structure can be improved.

"The disjoint wiring and reinforcement regions are recited in all of the independent claims 1, 6, and 9. Withdrawal of the rejection is requested."

(2) The wiring of Baba, regardless of being on or under the surface, does not meet another limitation of claim 1, namely, that it be in its own one of the claimed "mutually non-overlapping" regions (claims 1 and 6) or "mutually separated" regions (claim 9). The wiring of Baba is not illustrated and is not disclosed to be in any one region. To be covered by the Applicant's claims, it would need to be entirely in the narrow gap between the chip 1 and the reinforcement 6—which is clearly impossible if the wiring is to connect the solder balls 8 and 2.

This point was argued in the last response, but the Examiner has not responded to the argument.

The advantage of the Applicant's feature is that the reinforcement layers can be formed at the same time as the wirings, and additional manufacturing steps are not needed (no additional lithography). The prior art does not disclose or suggest this advantage.

(3) All of the independent claims now recite "a protective film that covers the wirings *and the reinforcement layer*." Claim 9 so recited previously.

The Examiner has not identified in this Action any element of Baba asserted to anticipate the Applicant's claimed reinforcement layer. However, the Action of May 5, 2005 did identify element 3 in Fig. 5D as assertedly anticipating it (page 2, next-to-last line), and identified the reinforcement as frame 6 (Action of May 5, 2005, fifth-from-last line). The Applicant replies based on the May 5 Action.

The applied figures clearly show that the asserted reinforcement layer 3 of Baba does not cover the asserted reinforcement layer 6 (Action of May 5, 2005, fifth-from-last line).

[§103–1] Claims 4, 7, and 10 were rejected under §103 over Baba in view of Lin. This rejection is respectfully traversed on the grounds set out above and the further grounds that planarizing Baba's layer 3 would destroy the chip 1, and also that the rejection has not established the advantage of reduced warpage and defects by either citation or reasoned argument.

[§103–2] Claims 5 and 8 were rejected under §103 over Baba in view of Norville. This rejection is respectfully traversed on the grounds set out above (both §§ 102 and 103).

[§103–3] Claim 11 was rejected under §103 over Baba in view of admitted prior art. This rejection is respectfully traversed on the grounds set out above.

[§103–4] Claims 14 and 19 were rejected under §103 over Baba in view of Niwa. This rejection is respectfully traversed on the grounds set out above.

Withdrawal of the rejections is requested.

Respectfully submitted,

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Date

Nick Bromer (Reg. No. 33,478)
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax : (202) 408-0924